## REMARKS

Claims 1-2 and 4-7 are pending in the application.

Claims 1-2 and 5-6 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **June 27, 2002**.

### Claim Rejections under 35 USC §112

Claims 1-6 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

The relevant claims have been amended, as needed, to overcome this rejection. Claim 3 is concurrently canceled herewith, rendering any rejection applied thereto moot.

Reconsideration and withdrawal of this rejection are respectfully requested.

### Claim Rejections under 35 USC §102

Claims 1, 2, 4 and 6 are rejected under 35 USC §102(e) as being anticipated by Liu (U.S. Patent No. 6,316,727).

In rejecting the claimed invention, the outstanding Office has specifically stated that:

> "Liu discloses ... a plate member 202 arranged on said first chip and having an end at an inward position of said first semiconductor chip from the pads;..."

We respectfully disagree. As clearly shown in Figure 2 of Liu, the lead frame 202 is centrally located relative to first chip 210 and second chip 222. The lead frame 202 is not at all having an end at an inward position of said first semiconductor chip from the pads, as alleged by the Office.

In contradistinction, as clearly shown in Figure 1 of the present invention, the plate member 20 is indeed arranged on first chip 18 and having an end at an inward position of said first semiconductor chip 18 from the pads 24.

To make these features even more distinct from Liu, independent claim 1 has been amended to recite:

> "1. (Amended) A semiconductor device comprising:
> a substrate having a first plurality of pads and a second plurality of pads;
> a first semiconductor chip mounted on said substrate and having a third plurality of pads;
> a plate member arranged on said first semiconductor chip [and] having [an] a first end at an inward position of said first semiconductor chip adjacent from the third plurality of pads, and a second end being exposed to an outside of a seal member through a side surface thereof;
> a second semiconductor chip arranged on said plate member [and] having a fourth plurality of pads;
> a first structure and a second structure respectively and electrically interconnecting said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and said fourth plurality of pads of said second semiconductor chip [to said pads] with said second plurality of pads of said substrate; and
> [a] the seal member sealing said first semiconductor chip and said second semiconductor chip."

As clearly shown in Figures 1-4 of the present invention, there is indeed shown a semiconductor device comprising a substrate 12 having a first plurality of pads 14 and a second plurality of pads 15; a first semiconductor chip 18 mounted on said substrate 12 and having a third plurality of pads 24; a plate member 20 arranged on said first semiconductor chip 18 having a first

end at an inward position of said first semiconductor chip 18 adjacent from the third plurality of pads 24, and a second end being exposed to an outside of a seal member 36 through a side surface 20a thereof; a second semiconductor chip 22 arranged on said plate member 20 having a fourth plurality of pads 26; a first structure 32 and a second structure 34 respectively and electrically inter-connecting said third plurality of pads 24 of said first semiconductor chip 18 with said first plurality of pads 14 of said substrate and said fourth plurality of pads 26 of said second semiconductor chip with said second plurality of pads 15 of said substrate 12; and the seal member 36 sealing said first semiconductor chip 18 and said second semiconductor chip 22.

In the arrangement of the amended claim 1, a plurality of semiconductor chips can be stacked in a package and the semiconductor chip can be cooled via the plate member which is exposed to the outside of the seal member. This would also allow moisture to be removed through the plate member.

The outstanding Office action further stated that:

> "Said plate having a first portion covered by first and second chips, and a second portion protruding from layers 228,218, wherein the second portion is flushed with a surface of the encapsulant 230."

We also respectfully disagree. As clearly depicted in Figure 2 of Liu, the lead frame 202 is entirely covered between first chip 210 and second chip 222. There is no depiction that any portion of lead frame 202 being protruded from die attaching material 218 and die attaching material 228. There is also no depiction that lead frame contain any second portion that is in a flush arrangement with a surface of encapsulant 230.

As also clearly shown in Figure 4 of the present invention, the plate member 20 indeed has a first portion covered by first chip 18 and second chip 22. There is also a second portion of plate member 20 that is in a flush arrangement with a surface 36a of sealing resin 36.

Again, to make these features even more distinct from Liu, claim 5 has been amended to recite:

> "5. (Amended) A semiconductor device according to claim 1, wherein said plate member includes a fifth plurality of pads and a sixth plurality of pads, [said] a third structure and a fourth structure respectively and electrically inter-connecting said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and said fourth plurality of pads of said second semiconductor chip [to] with said first plurality of pads of said substrate;
>
> wherein [includes members] a first member electrically connecting [at least one of] said fourth plurality of pads of said second semiconductor chip with said sixth plurality of pads of said plate member and a second member electrically connecting said fifth plurality of pads [of said second semiconductor chip] plate member with [to] said [pads of said plate member and members electrically connecting said pads of said plate member to said] second plurality of pads of said substrate."

As shown in Figures 1-4 of the present application, there is indeed shown a semiconductor device according to claim 1, wherein said plate member (20) includes a fifth plurality of pads (42) and a sixth plurality of pads (40), a third structure (32) and a fourth structure respectively and electrically inter-connecting said third plurality of pads (24) of said first semiconductor chip with said first plurality of pads (14) of said substrate and said fourth plurality of pads (26) of said second semiconductor chip with said first plurality of pads (14) of said substrate; wherein a first member (44) electrically connecting said fourth plurality of pads (26) of said second semiconductor chip with said sixth plurality of pads (40) of said plate member and a second member (46) electrically

connecting said fifth plurality of pads (42) of said second semiconductor chip plate member with said second plurality of pads (15) of said substrate.

These and other features of the claimed invention patentably distinguish the claimed invention from Liu.

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference. *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that independent claim 1, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as a column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

It is respectfully submitted that independent claim 1, as amended, patentably distinguishes over the asserted prior art. Claims dependent thereon, by the virtue of inherency, also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

**New Claim**

New claim 7 is added herein by amendment. Claim 7 is substantially the same as amended independent claim 1 differentiating therefrom in that "a second end being exposed to an outside of a seal member through a side surface thereof" is deleted and "a second end being flush with said semiconductor chip" is added. As clearly shown in Figure 1, indeed there is a second end being flush with said first semiconductor chip 18.

Entry and allowance of newly added claim 7 are respectfully requested.

**Conclusion**

In view of the aforementioned amendments and accompanying remarks, all pending claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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